REMARKS

In view of the following remarks, reconsideration and allowing of the above-referenced application is requested.

Claims 1-24 are pending with Claims 1, 7, 13, and 22 being independent. No new matter has been added.

Claims 1-24 stand rejected under 35 U.S.C. 102(b) as allegedly being anticipated by U.S. Patent No. 6,442,678 to Arora.

Claim 2 stands objected to for informalities. Claim 2 has been amended to remove a redundant "to the" to obviate the objection.

Claim 1

The amended Claim 1 is patentable over Arora for several reasons.

1. Claim 1 is not anticipated by Arora because the subject matter recited in Claim 1 is structurally different from Arora.

For example, the Arora teaches having a speculative register in the early stages of the pipeline, whereas the speculative commit register in Claim 1 is described as being in the last, or WB stage of the pipeline. Arora teaches that the instruction results written into pipeline latches 133, 135 at the same time as SRF 106 (Arora, Col. 4, lines 50-51). The SRF data doesn't come from the pipeline latches in the write back stage of the pipeline, instead the data are coming from the early stages of the pipeline (Arora, Col 2, lines 50-57). However, Claim 1 recites that the speculative commit register is written in the last, or WB stage of the pipeline. Therefore, Arora does not anticipate each and every feature of Claim 1.

In another structural difference, the Claim 1 recites "writing a value in the speculative commit register to an architectural register." As shown in Fig. 3 of the current disclosure, the output of the speculative commit register 302 is coupled to the input of the architectural register 304 (Fig. 3, paragraph 19 on pages 16-17). Arora does not describe this feature. Instead, Arora teaches that "an output of the architectural register file is coupled to an input of the speculative register file" (Arora, Abstract). Fig. 1 of Arora also shows that the output of the architectural register file 105 is coupled to the input of the speculative register file 106, and not teaching that the output of the speculative commit register is coupled to the input of the architectural register as supported in the current disclosure. Because of this structural difference, Arora does not anticipate "writing a value in the speculative commit register to an architectural register," as recited in Claim 1. For at least these structural differences with Arora, Claim 1 should be allowed.

2. Claim 1 is not anticipated by Arora at least because the subject matter recited in Claim 1 is functionally different from Arora.

For example, the use of "Multi-cycle instructions (MCIs)" as stated in the Office Action is different from MCIs as recited in Claim 1. Claim 1 recites "introducing a multi-cycle instruction including two or more sub-instructions into *multiple stages of a pipeline*." The MCI (multi-cycle instructions) not only may take multiple clock cycles to complete, but they also occupy multiple states of the pipeline concurrently to function as multi-stage instructions. Arora fails to anticipate this feature. Although Arora recites that any pipe stage may take any number of clock cycles (Arora, Col. 3, lines 7-8), Arora does not teach that the instructions occupy multiple pipe stages

concurrently. Instead, the Arora instructions only occupy a single pipe state at a time, and are not MCIs as described above and recited with respect to Claim 1.

In another functional difference, Arora teaches a different data flow for the feature of Claim 1. For example, Claim 1 recites that the writing of the value in the speculative commit register is to an architectural register - so, the direction of data is from the speculative commit register to the architectural register (Fig. 3 of disclosure, pages 6-7, paragraph 19). Because Arora is structurally different (e.g., different physical connections for a different data transfer) from the current disclosure, as described above, Arora cannot teach the same data flow as in Claim 1. Arora teaches that "the output of ARF 105 is coupled to an input of multiplexer 109," and the output of the multiplexer is coupled to the input of the SRF 106 (Arora, Col. 3, lines 20-28). Furthermore, Fig. 1 of Arora shows that the writing of the value in the speculative commit register is to either itself (via the mux 109) or to the first stage 101 of the pipeline.

Moreover, Arora teaches that speculative results become architectural results (Arora, Col. 5, lines 1-2). For instance, Arora teaches that pipeline latches are written into the architectural register specifically if the pipeline is not flushed. However, Claim 1 and the current disclosure teaches that data to the architectural register is not written from the pipeline latches, but from the speculative commit register. For at least these reasons, the Applicants submit that Claim 1 should be placed in condition for allowance.

In yet another functional difference that is not described in Arora, there is no unique behavior regarding the Arora SRF when encountering an instruction that could be regarded as a last or terminal sub-instruction. The Applicants contend that

the argument recited in the office action for Col. 1, lines 29-31 of Arora as the "last instruction is reasonable and broadly interpreted as a terminal sub-instruction" is incorrect based on, in part, Arora updating the ARF on every clock cycle for every instruction in the pipeline as long as a register result is produced. The Arora SRF behaves the same for every instruction, regardless of whether those instructions are regarded as conventional instructions or a sub-instruction. However, the speculative commit register, as recited in Claim 1, has unique behavior that occurs with the last or terminal sub-instruction that does not occur with earlier sub-instructions, (e.g., the "committing" and dependent Claims 3-4). Therefore, Claim 1 should be allowed for at least these functional differences.

3. Claim 1 is further patentable over Arora because Arora fails to anticipate each and every feature of the claim. For example, the Office Action fails to show where Arora teaches a single "commit" phase for an instruction that has all of the following elements: (1) multiple sub-instructions that are (2) spread across multiple states of the pipeline (3) concurrently.

Because the cited reference fails to anticipate each and every feature of the claim, and because Arora has structural and functional differences with the Claim 1 that are neither taught nor suggested, the Applicants contend that the 35 U.S.C. 102 rejection to Claim 1 should be respectfully withdrawn, and Claim 1 should be place in condition for allowance.

Claim 2-6

Applicants submit that Claims 2-6 are allowable because they depend from an allowable base claim, Claim 1, and are allowable for reciting allowable subject matter in their own right. Allowance of Claims 2-6 is respectfully requested.

Claim 7, 13, and 22

Claims 7, 13, and 22 recite one or more features that are similar to Claim 1, and are allowable for at least the same reasons as those of Claim 1.

For example, Claims 7, 13, and 22 all recite the functional difference that is not taught in Arora in that there is no unique behavior regarding the Arora SRF when encountering an instruction that could be regarded as a last or terminal sub-instruction. As described above, the Arora SRF behaves that same for every instruction whether or not those instructions are regarded as conventional instructions or a sub-instruction. For this functional reason and the other reasons mentioned above, the 35 U.S.C. 102 rejection to Claims 7, 13, and 22 should be respectfully withdrawn and these independent claims should be placed in condition for allowance.

Claims 8-12,14-21, 23-24

Applicants submit that Claims 8-12,14-21, 23-24 are allowable because they depend from an allowable base claim and are allowable for reciting allowable subject matter in their own right. Allowance of Claims 8-12,14-21, 23-24 is respectfully requested.

CONCLUSION

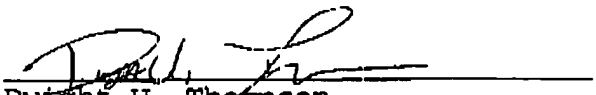
In view of the amendments and remarks, Applicants believe that all pending claims, Claims 1-24, are in condition for allowance and ask that those pending claims be allowed. The foregoing comments made with respect to the positions taken by the Examiner are not to be construed as acquiescence by the Applicants with other positions of the Examiner that have not been explicitly contested. Accordingly, Applicants' arguments

for patentability of a claim should not be construed as implying that there are not other valid reasons for patentability of that claim or other claims.

No fee is believed to be due at this time. Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: 10/22/04



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